Listing of Claims:

Please **cancel** claims 4-26 without prejudice.

Please **add** the following new claims:

27. (New) A method of forming a metal pattern, the method comprising:

forming an organometallic layer by coating a photosensitive organometallic complex;

exposing the organometallic layer to light through a photo mask; and

forming a final metal pattern directly from developing the organometallic layer.

28. (New) The method of claim 27 wherein the development of the organometallic layer is made by way of an organic solvent.

29. (New) The method of claim 27 wherein the light-blocking pattern of the photo mask is positioned at the area external to the area to be provided with the metal pattern.

30. (New) A method of manufacturing a thin film transistor array panel, the method comprising:

forming a gate wire on an insulating substrate, the gate wire including a gate line, a gate electrode and a gate pad;

sequentially depositing a gate insulating layer, an amorphous silicon layer and an ohmic contact layer on the gate wire;

patterning the ohmic contact layer and the amorphous silicon layer by photolithography; forming a data wire on the ohmic contact layer, the data wire including source and drain electrodes, a data line and a data pad;

forming a protective layer on the data wire, the protective layer having a first contact hole exposing the drain electrode, a second contact hole exposing the gate pad and a third contact hole exposing the data pad; and

forming a pixel electrode, a subsidiary gate pad and a subsidiary data pad on the protective layer, the pixel electrode being connected to the drain electrode through the first

contact hole, the subsidiary gate pad being connected to the gate pad through the second contact hole, the subsidiary data pad being connected to the data pad through the third contact hole;

wherein at least one of the formations of the gate wire, the data wire and the pixel electrode comprises:

forming an organometallic layer by coating a photosensitive organometallic complex;

placing a photo mask over the organometallic layer such that a predetermined region of the organometallic layer is exposed;

exposing the organometallic layer to light through a photo mask; and

developing the organometallic layer to thereby directly form at least one of the gate wire, the data wire and the pixel electrode.

31. (New) A method of manufacturing a thin film transistor array panel, the method comprising the steps of:

forming a gate wire on an insulating substrate, the gate wire having gate lines, gate electrodes and gate pads;

sequentially depositing a gate insulating layer, an amorphous silicon layer, an ohmic contact layer and a metallic layer on the gate wire;

patterning the metallic layer, the ohmic contact layer and the amorphous silicon layer by photolithography to form a data wire and channel portions, the data wire having source and drain electrodes, data lines and data pads, the channel portions being placed between the source and the drain electrodes;

forming a protective layer on the data wire, the protective layer having first to third contact holes; and

forming a pixel electrode, a subsidiary gate pad and a subsidiary data pad on the protective layer, the pixel electrode being connected to the drain electrode through the first contact hole, the subsidiary gate pad being connected to the gate pad through the second contact hole, the subsidiary data pad being connected to the data pad through the third contact hole;

wherein at least one of the steps of forming the gate wire, the data wire and the pixel electrode comprises the sub-steps of:

forming an organometallic layer by coating a photosensitive organometallic complex;

placing a photo mask over the organometallic layer such that a predetermined region of the organometallic layer is exposed to the outside;

exposing the organometallic layer to light by the photo mask; and

developing the organometallic layer to thereby directly form at least one of the gate wire, the data wire and the pixel electrode.

32. (New) The method of claim 30 or 31 wherein the development of the organometallic layer is made by way of an organic solvent.

33. (New) The method of claim 30 or 31 wherein the light-blocking pattern of the photo mask is positioned at the area external to the area to be made of the signal wire or the pixel electrode.

34. (New) The method of claim 30 or 31 wherein the metal is Ag.

35. (New) The method of claim 30 or 31 wherein the protective layer has a surface with prominent and depressed portions.

36. (New) A thin film transistor array panel comprising:

an insulating substrate;

a gate wire formed on the insulating substrate;

a gate insulating layer formed on the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the semiconductor layer and the gate insulating layer;

a protective layer formed on the data wire; and

a pixel electrode formed on the protective layer;

wherein at least one of the gate wire, the data wire and the pixel electrode is formed by way of a metal pattern formation process comprising the steps of:

forming an organometallic layer by coating a photosensitive organometallic complex;

placing a photo mask over the organometallic layer such that a predetermined region of the organometallic layer is exposed to the outside;

exposing the organometallic layer to light through the photo mask; and

developing the organometallic layer to thereby directly form at least one of the gate wire, the data wire and the pixel electrode.

37. (New) The thin film transistor array panel of claim 36 wherein the semiconductor layer comprises an amorphous silicon layer and an ohmic contact layer, the ohmic contact layer has the same plane pattern as the data wire, and the amorphous silicon layer has the same plane pattern as the ohmic contact layer at the non-channel area.

38. (New) A thin film transistor array panel comprising:

an insulating substrate;

a gate wire formed on the insulating substrate;

a gate insulating layer formed on the gate wire;

a data wire formed on the gate insulating layer with a triple-layered structure of an amorphous silicon layer, an ohmic contact layer and a metallic layer;

a protective layer formed on the data wire; and

a pixel electrode formed on the protective layer;

wherein at least one of the gate wire, the data wire and the pixel electrode is formed by way of a metal pattern formation process comprising the steps of:

forming an organometallic layer by coating a photosensitive organometallic complex;

placing a photo mask over the organometallic layer such that a predetermined region of the organometallic layer is exposed to the outside;

exposing the organometallic layer to light through the photo mask; and

developing the organometallic layer to thereby directly form at least one of the gate wire, the data wire and the pixel electrode.

39. (New) The thin film transistor array panel of claim 38 wherein the data wire has data lines, source electrodes connected to the data lines and drain electrodes facing the source electrodes, and a channel portion is formed between the source and the drain electrodes only with an amorphous silicon layer.